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14. ABSTRACT Our first-generation electronic microsystem is tested successfully in an anesthetized rat model by recording neural spikes from the somatosensory cortex of the brain, and stimulating the primary motor cortex that results in clear wrist movements. Using a controlled cortical-impact device, we have successfully induced traumatic brain injury (TBI) in the caudal forelimb area of the rat brain, sparing the rostral forelimb area that is the target for implantation of the electronic microsystem. We have demonstrated that a wide range of impact parameters satisfy the requirements of the study for post-TBI implantation of the device. Behavioral assessments of reaching, retrieval of small food items, and locomotion demonstrate that deficits persist during the 5-week recovery period following injury. This will provide us with an ideal time window during which to test the effects of the device after injury.					
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Implantable Microsystems for Anatomical Rewiring of Cortical Circuitry: A New Approach for Brain Repair

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Introduction

The overall goals of this project are to shape long-range intracortical connectivity patterns by driving coupling of activity between distant cortical locations. Over the past several years, it has been demonstrated that after a stroke-like lesion in the cerebral cortex of non-human primates, the remaining intact tissue undergoes extensive neurophysiological and neuroanatomical remodeling. Researchers have recently demonstrated the remarkable ability of cortical areas remote from the infarct to form new cortico-cortical connections over long distances between the frontal and parietal lobes. It is likely that these novel connections play a role in functional recovery after cortical injury. In this project, we combine neurobiological tools with state-of-the-art implantable device technology to develop a novel microsystem that will be used to guide post-injury axonal sprouting in order to reshape cortical connections, optimize connectivity patterns, and hence improve long-term functional recovery after a traumatic brain injury (TBI). We will capitalize on recent advancements in designing neuroprosthetic devices to temporally couple the activity of remote cortical locations that are not normally co-activated or interconnected, taking advantage of the injured brain's ability to produce growth-promoting substances that encourage anatomical rewiring. We hypothesize that such temporal coupling will encourage growing axons to migrate toward and terminate in the coupled region. The results of this initial study in rodents will be used to design a subsequent series of experiments to determine if this approach can be used in non-human primate models of injury, and whether such artificially generated rewiring results in improved functional recovery after TBI.

Body

In this section of the annual report, we describe the research accomplishments associated with each task outlined in the approved Statement of Work.

1. Electronics

For **Tasks 1.1** and **1.2**, a fully integrated neural recording front-end comprising a low-noise two-stage amplification circuitry and a 10-bit successive approximation register (SAR)-based analog-to-digital converter (ADC) was fabricated using the TSMC 0.35 μ m 2P/4M n-well CMOS process. The ac-coupled amplification circuitry provided a maximum mid-band ac gain of 52 dB and featured a measured input-referred voltage noise of 3.5 μ V_{rms} from 0.1 Hz to 12.8 kHz, while dissipating 78 μ W from 2 V. The SAR ADC featured an effective number of bits (ENOB) of 9.4 for maximum sampling frequency of 45 kSa/s, while dissipating only 16 μ W. Details of design considerations, circuit architectures, and *in vitro* measurement results can be found in Appendix I (Azin and Mohseni, *BioCAS'08*, pp. 221-224, November 2008).

For **Task 1.3**, monolithic circuitry was designed using standard digital cells to identify the presence of large action potentials in the recorded digitized data with a spike discrimination algorithm based on two programmable threshold levels and time-amplitude windows. Detected spikes were then used to trigger the back-end microstimulator with a programmable delay. A first-order digital highpass filter was also designed to remove any dc/low-frequency signal components prior to spike discrimination. The measured power consumption was less than 1 μ W with a 1.5-V supply and ADC sampling frequency of 35 kSa/s.

For **Task 1.4**, a high-output-impedance current microstimulator was fabricated using the TSMC 0.35 μ m CMOS process. It delivered a maximum current of 94.5 μ A to the target cortical tissue with current efficiency of

86% and voltage compliance of 4.7 V with a 5-V supply. The stimulus current could be programmed via a 6-bit digital-to-analog converter (DAC) with accuracy better than 0.47 LSB. Details of design considerations, microstimulator architecture, and *in vitro* measurement results using a silicon microelectrode with iridium oxide (IrO) stimulation sites can be found in Appendix II (Azin and Mohseni, *ISCAS'08*, pp. 2502-2505, May 2008).

For **Task 1.5**, we developed a cross-coupled voltage-controlled oscillator (VCO) for digital frequency-shift-keyed (FSK) transmission based on an earlier design that was developed in PI Mohseni's laboratory for a different project. The oscillator tank employed a surface-mount, high-Q, off-chip inductor for low-power operation at a frequency near 433 MHz. The tank varactors were implemented using PMOS capacitors with source/drain/bulk connected to each other. To have flexibility in selecting a suitable ΔF for the FSK transmitter, the varactors were divided into two sets of binary-weighted capacitors that could be externally controlled with three bits. Using this tuning scheme, ΔF could be varied in the range of 2-14 MHz in steps of 2 MHz. Details of design considerations, transmitter architecture, and measurement results can be found in Section III.B of Appendix III (Roham, et al., *Trans. Biomed. Eng.*, pp. 2628-2634, November 2008).

For **Task 1.6**, as stated above, all electronic circuitry was fabricated using the TSMC 0.35 μ m 2P/4M n-well CMOS process, measuring 2.6×2.6 mm². A microphotograph of the fabricated chip is shown in both Appendices I & II.

2. Microsystem Packaging

For **Task 2.1**, a comparative study was performed among four different monopolar and bipolar electrodes for use in intracortical microstimulation (ICMS). The purpose of the study was to determine if the type of electrode used for ICMS would affect the properties of the stimulation. A concentric electrode from Nano BioSensors (Nazareth, Israel), concentric and matrix electrodes from FHC (Bowdoin, ME), and a "Michigan" silicon-substrate electrode from NeuroNexus (Ann Arbor, MI) were compared *in vivo* in an anesthetized rat model based on the current threshold needed to drive a joint movement and the areal representation of the forelimb areas. In the case of the "Michigan" electrode, electrochemical polymerization of the stimulating sites with poly (3, 4-ethylenedioxythiophene) (PEDOT) nanotubes was performed to significantly reduce the site impedance and increase the charge transfer capacity during stimulation [1].

Details of the experimentation methodology and measured results in this comparative study can be found in Appendix IV (Guggenmos, et al., *Neuroscience Symposium*, November 2008). In summary, the PEDOT-activated "Michigan" electrode showed similar thresholds and map areas, but had significantly lower impedance values compared to the other electrodes. In addition, it had a smaller tip size compared to the other bipolar electrodes used. The activated "Michigan" electrode would therefore be the most appropriate choice of those tested for our application.

Work is still ongoing for **Tasks 2.2 – 2.5** in the *Microsystem Packaging* research thrust. We have already identified a commercial manufacturer for fabricating rigid and flexible (polyimide) substrates. Flexible Circuit Technologies (Plymouth, MN) is a leading supplier of flexible and rigid/flex circuits for a wide variety of applications. We have also identified ProtoConnect (Ann Arbor, MI) for die attachment, encapsulation, wire bonding, and electrode connection to the flexible substrate for microsystem assembly and packaging.

3. Neurobiology

For **Task 3.1**, neurophysiological procedures were conducted to record spontaneous activity in the rostral forelimb area (RFA) of intact, ketamine-anesthetized rats. Since spontaneous activity is particularly high under this anesthetic, we were able to record several seconds of neuronal activity with adequate signal-to-noise ratio. The digitized data was provided to PI Mohseni to use for modeling detection and control algorithms. The concentric and matrix electrodes were used in these studies, because the "Michigan" electrodes were not yet available. However, subsequent neuronal recordings with the "Michigan" electrodes have demonstrated superior recording characteristics in the form of substantially reduced noise.

For **Task 3.2**, we assessed behavioral measures of forelimb use in intact rats using a reach/retrieval task and a foot-fault test. In the reach/retrieval task, rats were placed in a Plexiglas behavioral testing chamber, and

then required to reach with one forepaw through a slot to retrieve a flavored pellet placed on a platform outside of the chamber. After 5 days of shaping (10 min per day), we acquired baseline performance data during daily 20-min sessions for two weeks. From video records, we quantified successful retrievals, drops, and percentage of successful trials. Five of six rats met our pre-determined inclusion criterion of >50% success. Among those five rats, the average percentage of successful retrievals was 76%. In the foot-fault test, rats were required to ambulate across a platform with a 5-cm grid opening for 2 min. The number of slips made with the forelimbs or hindlimbs was recorded using frame-by-frame analysis. A forelimb placement score was calculated by the percentage of slips made by the limb of interest divided by the total number of steps. Average foot-faults for the group made by the forelimbs was 18%; average by the hindlimbs was 27%. An asymmetry score was obtained by dividing the slips made on one side from the slips made on the opposite side. Forelimb asymmetry for the group was 1.05 (right slips/left slips), while hindlimb asymmetry was 1.24 (right slips/left slips).

For **Task 3.3**, we used microstimulation techniques in ketamine-anesthetized rats to determine the location and extent of the caudal and rostral forelimb areas. From these data, we can predict the location of caudal forelimb area relative to stereotaxic coordinates with a high degree of accuracy. These coordinates will be used in Phase II in locating the center of the TBI impact. A portion of the results was reported in abstract form (Bury, et al., *Neuroscience Symposium*, November 2008).

For **Task 3.4**, we conducted an optimization study to determine the parameters for the controlled cortical-impact (CCI) device. The goal was to produce a focal TBI injury in the caudal forelimb area that resulted in chronic motor deficits for at least several weeks, but that spared the rostral forelimb area, the target for the implantable device. Six rats were assigned randomly to 3 CCI groups. CCI-1 received focal cortical injury using a 3-mm diameter round impact tip; CCI-2 employed a 3.25-mm diameter flat impact tip; CCI-3 employed a 3.25-mm diameter round impact tip. Behavioral results demonstrated that skilled reach and contralateral foot-faults were impaired throughout the 5-week recovery period. However, no differences were found among the different groups. Microstimulation experiments confirmed that the CFA was destroyed to varying extents in all animals, while the RFA was spared by the delivered contusion, as intended. The post-mortem histology obtained from each impact group demonstrated that all lesions were observed in motor cortex and down through all the cortical layers. We conclude that the parameters used for controlled cortical impact are adequate for the Phase II studies, and that the various tip configurations do not substantially affect the outcomes.

For **Task 3.5**, all the regulatory review and approval processes for animal studies were conducted prior to the award activation date. Manuscripts for the Neurobiology tasks are now in preparation.

Key Research Accomplishments

- Design and fabrication of integrated neural recording front-end incorporating amplification and digitization.
- Demonstration of *in vivo* functionality of front-end by recording neural spikes from somatosensory cortex of anesthetized rat.
- Design and fabrication of integrated neural microstimulator.
- Demonstration of *in vivo* functionality of microstimulator by driving wrist movement after stimulating primary motor cortex of anesthetized rat.
- Design and fabrication of very-low-power digital filtering and spike discrimination circuitry.
- Results from a comparative study among various monopolar and bipolar electrodes for intracortical microstimulation.
- Demonstration of the reliability of baseline motor behaviors in intact rats, including stable reach/retrieval and foot-fault performance.
- Demonstration of the ability of a focal controlled cortical impact limited to the caudal forelimb area to produce significant chronic deficits in motor performance in rats.
- Demonstration that a wide range of impact parameters satisfy the requirements of the study for post-TBI implantation of the electronic microsystem.

Reportable Outcomes

1- Manuscripts/Abstracts/Presentations:

- M. Azin and P. Mohseni, "A 94- μ W 10-b neural recording front-end for an implantable brain-machine-brain interface device," in *Proc. IEEE Biomed. Circuits and Systems Conf. (BioCAS'08)*, pp. 221-224, Baltimore, MD, November 20-22, 2008.
- D. J. Guggenmos, S. Barbay, P. Mohseni, and R. J. Nudo, "A comparison of monopolar and bipolar electrodes for use in intracortical microstimulation," *Program No. 101.23, Neuroscience Meeting Planner*, Washington, DC, Society for Neuroscience, November 2008.
- S. D. Bury, E. T. Urban, III, S. Barbay, E. J. Plautz, and R. J. Nudo, "Characterization of cortico-cortical projections from the rostral forelimb area to the caudal forelimb area in the rat," *Program No. 78.16, Neuroscience Meeting Planner*, Washington, DC: Society for Neuroscience, November 2008.
- M. Azin and P. Mohseni, "A high-output-impedance current microstimulator for anatomical rewiring of cortical circuitry," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'08)*, pp. 2502-2505, Seattle, WA, May 18-21, 2008.
- M. Azin, E. T. Urban, III, R. J. Nudo, and P. Mohseni, "Implantable microsystems for anatomical rewiring of cortical circuitry," *38th Neural Interfaces Conf. (NIC'08)*, Cleveland, OH, June 16-18, 2008.
- P. Mohseni, "Wireless integrated devices for brain monitoring and stimulation," *Dept. of Electrical and Computer Engineering, University of Texas-Austin*, Austin, TX, March 20, 2008.

2- Patents and Licenses Applied for/Issued: None yet.

3- Degrees Obtained from Award: None yet.

4- Development of Cell Lines and Tissue/Serum Repositories: Not applicable.

5- Infomatics (Databases and Animal Models): None yet.

6- Funding Applied for:

- *Anatomical Rewiring of Cortical Circuitry for Functional Recovery after Stroke*; American Heart Association; PI Mohseni and Co-I Nudo; \$131,983; 2009-2011 (Pending).
- *EFRI-BSBA Preliminary Proposal: Smart Prosthetic Platforms for Altering Brain Plasticity*; NSF-EFRI; PI Mohseni and Co-PIs Nudo/Mastrangelo; \$1,998,079; 2009-2013 (Declined).

7- Employment/Research Opportunities Applied for/Received: None yet.

Conclusion

In conclusion, rapid progress is being made toward developing smart prosthetic platforms for altering plasticity in the injured brain, leading to future therapeutic interventions for TBI that are guided by the underlying mechanisms for long-range functional and structural plasticity in the cerebral cortex. Our first-generation integrated device was tested successfully in an anesthetized rat model by recording neural spikes from the somatosensory cortex of the brain, and stimulating the primary motor cortex that resulted in clear wrist movements. Using a controlled cortical-impact device, we have successfully induced TBI in the CFA, sparing the RFA. Behavioral assessments of reaching, retrieval of small food items, and locomotion demonstrate that deficits persist during the 5-week recovery period following injury. Work is still ongoing for system assembly and packaging in the form of a miniature implantable device to test our hypothesis on long-range intracortical connectivity formation post TBI during the remaining grant performance period.

References

[1] Abidian MR, Martin DC (2008) Experimental and theoretical characterization of implantable neural microelectrodes modified with conductive polymer nanotubes. *Biomaterials*, 29, 1273-1283.

Appendix I M. Azin and P. Mohseni, “A 94- μ W 10-b neural recording front-end for an implantable brain-machine-brain interface device,” in *Proc. IEEE Biomed. Circuits and Systems Conf. (BioCAS’08)*, pp. 221-224, Baltimore, MD, November 20-22, 2008.

A 94- μ W 10-b Neural Recording Front-End for an Implantable Brain-Machine-Brain Interface Device

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Abstract-This paper describes a fully integrated neural recording front-end comprising a low-noise two-stage amplification circuitry and a 10-b successive approximation register (SAR)-based ADC as part of a fully implantable brain-machine-brain interface (BMBI) device for neuroanatomical rewiring of cortical circuitry in an injured brain. Fabricated using the TSMC 0.35 μ m 2P/4M n-well CMOS process, the ac-coupled amplification circuitry provides a maximum mid-band ac gain of -52 dB and features a measured input-referred voltage noise of 3.5 μ V_{rms} from 0.1 Hz to 12.8 kHz, while dissipating ~78 μ W from 2 V. The SAR ADC features an ENOB of ~9.4 for maximum sampling frequency of ~45 kSa/s, while dissipating only 16 μ W. Benchtop as well as *in vitro* measurement results in saline are reported.

Index Terms-Brain-machine-brain interface, Neural recording, Neuroanatomical rewiring, Neurostimulation.

I. INTRODUCTION

Throughout an individual's life, a brain cell's connections branch and proliferate, and the communication between brain cells is modulated within a complex network. Thus, it is not surprising that after an injury to cerebral cortex the structure and function of brain cells and their interconnections is drastically altered. Since brain plasticity may contribute to neuro-rehabilitation after brain injury, it is critical to understand how plasticity patterns might be directed to optimize motor function recovery.

Recent studies have demonstrated that both local (i.e., short-range) and long-range axonal sprouting spontaneously occur in the intact tissue adjacent to a focal cortical injury [1], [2]. Moreover, functional relationships have been built into intact adult nervous system by artificially driving temporal sequences of inputs and outputs of two cortical modules over short distances (i.e., 1-2 mm) using an autonomous head-mounted electronic device made in discrete fashion using commercial off-the-shelf components. Following several days of device entrainment, the two disparate cortical modules had similar motor output properties [3].

In this work, we aim to combine neurobiological tools with state-of-the-art implantable device technology to examine *neuroanatomical* changes over much longer distances (> 1 cm) in an injured brain model. More specifically, we aim to develop a fully integrated brain-machine-brain interface (BMBI) device to temporally couple the activity of remote cortical locations that are not normally co-activated or interconnected. We hypothesize that such temporal coupling

encourages the growing axons to migrate toward and terminate in the coupled region, as conceptually illustrated in Fig. 1, effectively bypassing the injured location in the brain.

Fig. 2 shows the block diagram of the proposed system architecture. The front-end amplifier provides on-chip ac amplification, dc baseline stabilization, and bandpass filtering to the extracellular neural signals recorded by a microelectrode placed in one area of the cortex. A successive approximation register (SAR)-based ADC digitizes the amplified neural signals with 10 bits of resolution. A low-power monolithic digital signal processing (DSP) unit provides additional filtering, and subsequently identifies the presence of large single-unit action potentials in the recorded data based on threshold crossing and programmable time-amplitude windows, executing a spike discrimination algorithm. The detected action potentials are then used to trigger a back-end cortical stimulator to drive a second microelectrode placed in the target area with stimulus current pulses of up to ~100 μ A.

This paper reports on the design, implementation, benchtop characterization, and *in vitro* testing of the analog/mixed-signal recording front-end of the BMBI device fabricated using a 0.35- μ m standard CMOS process.

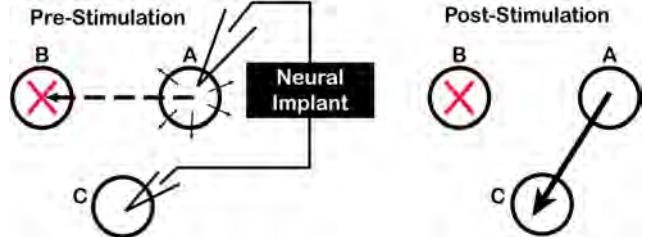


Fig. 1. Hypothetical effects of activity-dependent stimulation on long-range intracortical connectivity. Left: After injury to B, normal connections are lost (dashed arrow). Post-injury growth proteins induce local axonal sprouting (short arrows). Neural implant will drive synchronous activity between A and C. Right: New anatomical connections form between A and C.

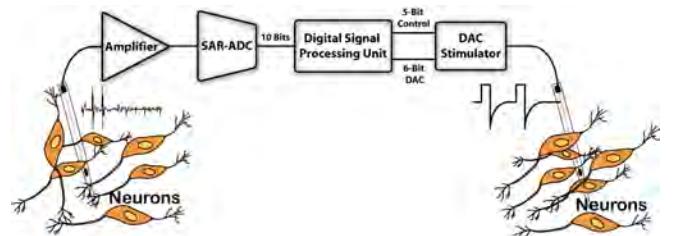


Fig. 2. Schematic block diagram of the proposed integrated neural implant for activity-dependent intracortical microstimulation.

II. DESIGN CONSIDERATIONS

The neural recording front-end consists of a two-stage (primary and secondary) amplification circuitry followed by a SAR ADC. Due to the low-level amplitude of extracellular neural spikes ($50\text{-}500 \mu\text{V}_{\text{pp}}$, with $100 \mu\text{V}_{\text{pp}}$ being fairly typical [4]), low-noise integrated circuits have to amplify the weak neural signals before any further signal processing can be performed. In most neural recording applications the total input-referred noise, comprising the electrode thermal noise (dependent on site impedance and recording BW), neural background noise, and interface electronics noise, is kept below $\sim 20 \mu\text{V}_{\text{rms}}$ in the neural frequency range of $0.1\text{-}10 \text{ kHz}$ [4]. Given a typical recording site impedance of a few megohms at 1 kHz , this further necessitates that the total interface electronics noise (amplifier's thermal/flicker noise and ADC's quantization noise) be kept below $\sim 10 \mu\text{V}_{\text{rms}}$.

Fig. 3 shows the schematic block diagram of the neural recording amplification circuitry, consisting of a low-noise primary amplifier followed by a variable-gain secondary amplifier with rail-to-rail output swing. The ac-coupled primary amplifier is designed to provide a stable mid-band ac gain of $\sim 32 \text{ dB}$ set by the capacitive ratio of C_1/C_2 . Furthermore, capacitor C_2 (0.75-pF on-chip double-poly capacitor) in conjunction with pseudo-resistive MOS-bipolar devices (M_{s1-2} , [5]) set the low cutoff frequency of the bandpass response at $\sim 1 \text{ Hz}$ to remove dc and low-frequency drift voltages at the electrode-electrolyte interface. Additional filtering is envisioned to be performed by the DSP unit (see Fig. 2) to accurately set the low cutoff frequency of the overall channel at $\sim 100 \text{ Hz}$ for detecting action potentials. The primary amplifier frequency response is band-limited at $\sim 10 \text{ kHz}$ by the on-chip capacitor C_C ($\sim 20 \text{ pF}$) to reduce thermal noise. To maintain symmetry and minimize the impact of bias-circuit-induced noise, additional capacitors (C_{3-4}) and pseudo-resistive devices (M_{s3-4}) are employed identical to those connected to the inverting input terminal.

III. FRONT-END CIRCUIT ARCHITECTURE

A. Primary Amplifier

The low-noise primary amplifier employs a folded-cascode topology as shown schematically in Fig. 4. Transistors M_{11-12} are added to further increase the open-loop gain and closed-loop linearity. The noise contribution of transistors M_{5-12} is minimized given the selected topology and their bias current levels. Given that PMOS transistors in general have less flicker noise compared to that of their NMOS counterparts in a standard CMOS process (by one order of magnitude or more as long as the gate overdrive voltage is not too high) [6], large PMOS input transistors (M_{1-2} , $W/L = 800 \mu\text{m}/4 \mu\text{m}$) are employed in this work, operating in the weak inversion region to provide a high g_m/I_D ratio. Transistors M_{3-4} ($W/L = 2 \mu\text{m}/20 \mu\text{m}$) are biased in the strong inversion region to further minimize their contribution to the input-referred noise. Further reduction of their sizing is limited by the available power supply and output node voltage swing range.

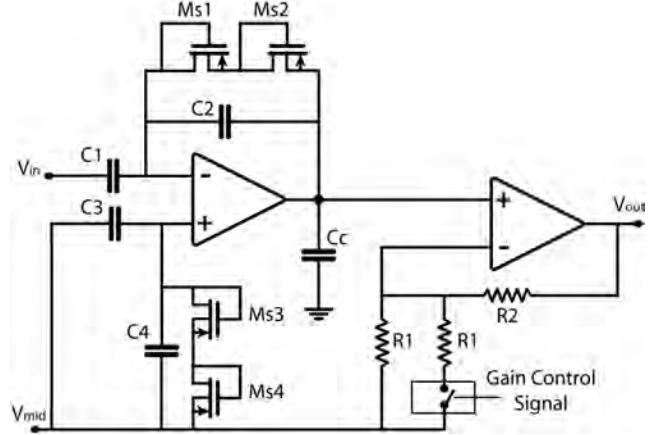


Fig. 3. Schematic block diagram of the front-end amplification circuitry.

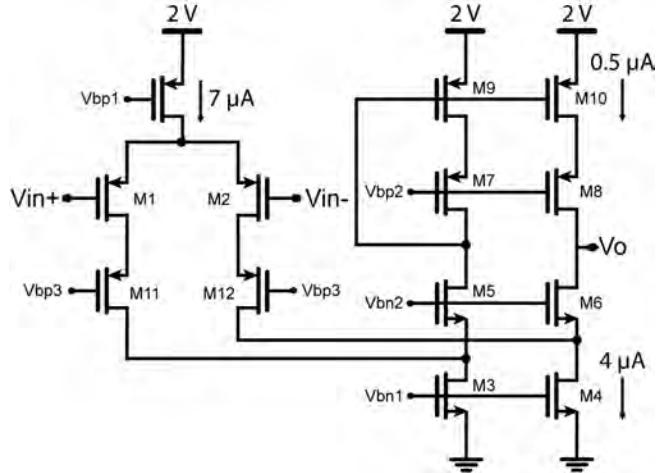


Fig. 4. Transistor-level circuit schematic of the low-noise primary amplifier.

B. Secondary Amplifier

The variable-gain secondary amplifier with rail-to-rail output swing employs a standard 2-stage CMOS op-amp topology in resistive feedback configuration to provide an additional gain of either $\sim 15 \text{ dB}$ or 20 dB , depending on the status of the externally applied gain control signal. Feedback resistors implemented using polycidied polysilicon layer are employed instead of capacitive and pseudo-resistive MOS-bipolar elements to alleviate nonlinearity concerns arising from large voltage swing of the output node. The secondary amplifier draws $\sim 9 \mu\text{A}$ from a 2-V power supply, and has adequate current drive capability to charge/discharge the capacitor network of the subsequent SAR ADC.

C. Successive Approximation Register ADC

For analog-to-digital conversion, a SAR-based ADC with a capacitor network is used due to its low power consumption, as shown in Fig. 5. During the sampling period (16 clock cycles), the capacitor network is connected between the amplifier output (i.e., ADC input, V_{in}) and the positive reference voltage ($V_{\text{ref-P}}$).

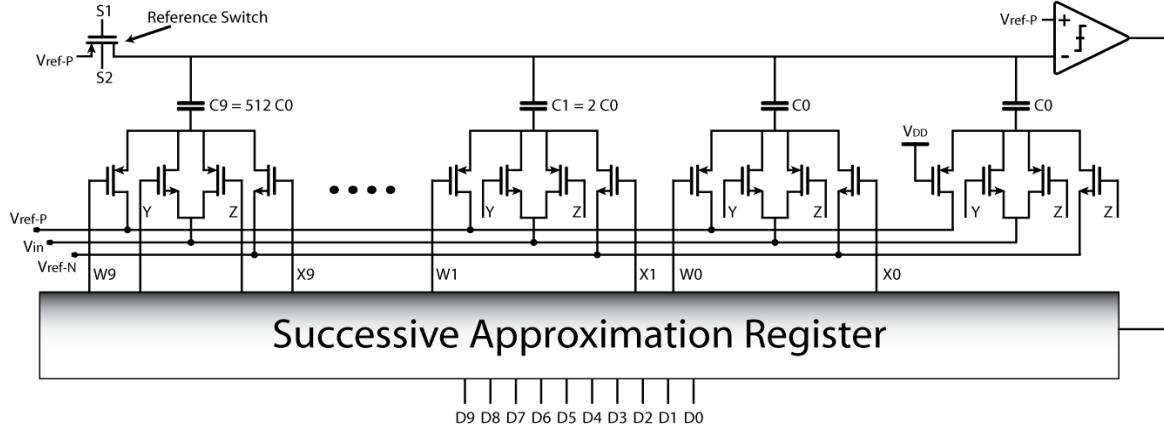


Fig. 5. Schematic block diagram of the SAR ADC.

Prior to the approximation period, all eleven capacitors will be held at the negative reference voltage (V_{ref-N}) for one clock cycle. Next, the largest capacitor, C_9 , will be connected to V_{ref-P} and the comparator output will determine whether the ADC input voltage is larger than $0.5 \times (V_{ref-P} + V_{ref-N})$. If larger, capacitor C_9 will remain connected to V_{ref-P} ; otherwise it will be connected to V_{ref-N} . This sequence will be repeated for all the other capacitors to determine the subsequent bits. Therefore, the approximation period lasts for 10 clock cycles. After one additional cycle of reset, the output sample is ready after a total of 28 clock cycles.

The main tradeoff in ADC design for this application is between the power consumption and accuracy, predominantly determined by the unit capacitor size (~15 fF). Capacitor mismatch strongly affects ADC linearity; the larger the unit capacitor the better the matching. However, increasing the unit capacitor size increases the dynamic power consumption of the capacitor network as well as the power consumption in the secondary amplifier needed to drive a larger capacitive load.

A very-low-power (dc current draw of $\sim 1.5 \mu\text{A}$) latched comparator is utilized in the ADC architecture, as shown in Fig. 6. When the clock signal is high, a small voltage difference at the comparator input terminals leads into a corresponding difference between drain currents of M_{5-6} . When the clock signal goes low, the bi-stable network of $M_5 \sim M_8$ assumes one of its two stable states based on the drain current difference in M_{5-6} . The latch circuit will be then activated after a short delay of ~ 150 ns to hold the comparator output for the next clock cycle. The time delay allows the comparator output voltages V_{1-2} to settle to their final values before the latch is activated.

IV. MEASUREMENT RESULTS

A prototype chip was fabricated using the TSMC 0.35 μm 2P/4M n-well CMOS process, as shown in Fig. 7. The chip contained the front-end recording circuitry described herein as well as the back-end current microstimulator described in [7]. In future generations of the device, we plan to also incorporate a low-power DSP unit for additional filtering as well as neural signal processing for spike discrimination.

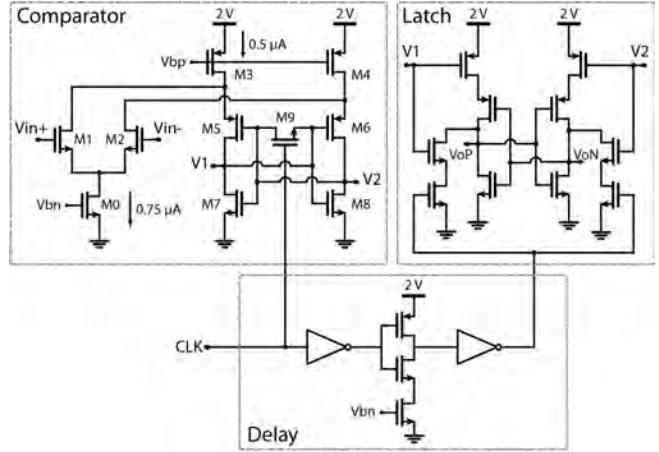


Fig. 6. Transistor-level circuit schematic of the latched comparator.

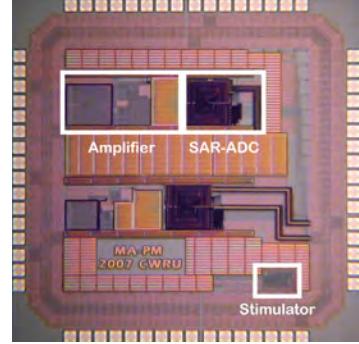


Fig. 7. Microphotograph of the fabricated chip.

Fig. 8 shows the measured input-referred voltage noise of the front-end amplification circuitry including both primary and secondary stages. The total input noise was measured to be $\sim 3.5 \mu\text{V}_{\text{rms}}$ within the measured amplification bandwidth of 0.1 Hz to 12.8 kHz while dissipating $\sim 77.6 \mu\text{W}$ from a 2-V supply. Given a total core current draw of 8 μA in the primary amplifier, the noise efficiency factor (NEF) [5] is found to be 3.4, which is one of the lowest reported NEF values for biopotential recording amplifiers.

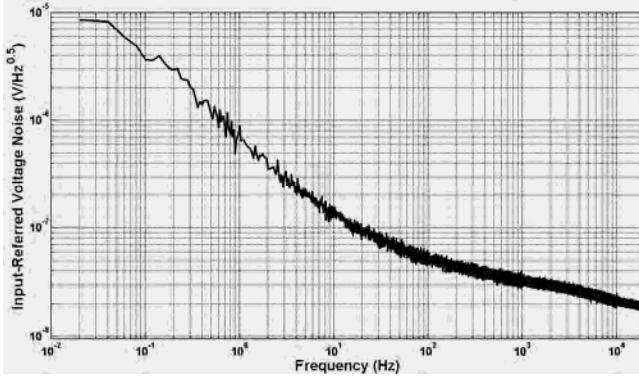


Fig. 8. Measured input-referred voltage noise of the front-end amplification circuitry.

The SAR ADC had a measured ENOB of ~ 9.4 for clock frequencies up to 1.25 MHz, providing a maximum sampling frequency of ~ 45 kSa/s (adequate for single-channel detection of action potentials) while dissipating only 16 μ W from a 2-V supply. According to Fig. 9, the measured INL_{max} and DNL_{max} were 0.8 and 0.9 LSB, respectively. Table I summarizes the measured benchtop performance of the recording front-end.

For further *in vitro* experiments in saline, the CMOS chip was interfaced with a silicon-substrate neural recording electrode with recording sites of iridium having an area of $\sim 177 \mu\text{m}^2$ and impedance magnitude of $\sim 2 \text{ M}\Omega \angle -81^\circ$ at 1 kHz. A 20-ms snapshot of pre-recorded neural activity, evoked by an acoustic white-noise burst from the inferior colliculus of a guinea pig and containing two distinguishable μV -range neural action potentials, was applied to saline solution via a large platinum electrode. Fig. 10 depicts the input-referred signal measured at the output of the ADC with no additional offline filtering applied. Total gain was ~ 52 dB.

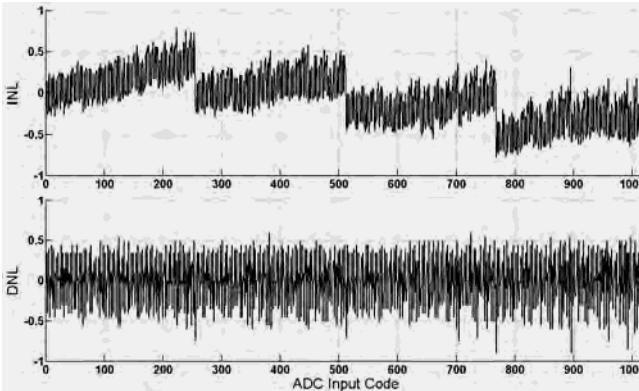


Fig. 9. Measured INL and DNL of the SAR ADC.

V. CONCLUSION

We have developed a fully integrated neural recording front-end as part of an implantable device for activity-dependent intracortical microstimulation. The ac-coupled amplifier provides a maximum gain of ~ 52 dB from 0.1 Hz to 12.8 kHz while dissipating $\sim 78 \mu\text{W}$ from a 2-V power supply.

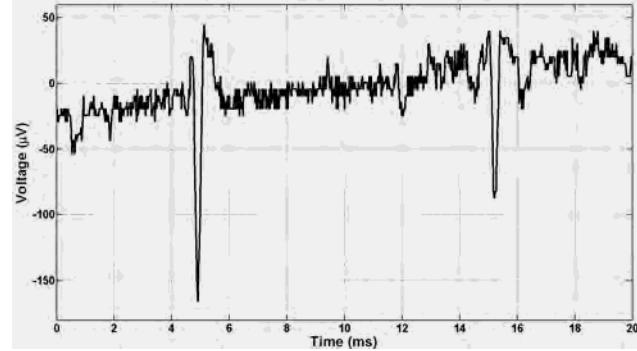


Fig. 10. Input-referred signal measured at the ADC output in an *in vitro* experiment. The smaller action potential had amplitude of 127 μV_{pp} (26 LSB).

TABLE I
SUMMARY OF MEASURED CHIP PERFORMANCE

Amplifier Gain	51.99 dB ± 0.01 dB
Amplifier BW	0.1 Hz – 12.8 kHz
Amplifier Input-Referred Noise	2.6 μV_{rms} (0.1 – 10 kHz) 3.5 μV_{rms} (0.1 Hz – 12.8 kHz)
Amplifier Power Consumption	77.6 μW (@ 2 V)
Noise Efficiency Factor	3.4
Amplifier THD (4.8-mV _{pp} Sinusoidal Input and Gain = 52 dB)	-43 dB @ 1 Hz -66 dB @ 100 Hz -60 dB @ 1 kHz
Amplifier PSRR	52 dB @ 1 kHz
ADC ENOB	~ 9.4 ($f_{\text{CLK}} = 1.25$ MHz ; $f_{\text{in}} = 1$ kHz)
ADC Maximum Sampling Rate	~ 45 kSa/s ($f_{\text{CLK}} = 1.25$ MHz)
ADC Maximum Nonlinearity	INL = 0.8 LSB ; DNL = 0.9 LSB
ADC Power Consumption	16 μW (@ 2 V and 1.25 MHz)

The 10-b SAR ADC exhibits a measured ENOB of ~ 9.4 for sampling frequencies up to ~ 45 kSa/s, while dissipating only 16 μW when clocked at 1.25 MHz. The performance of the neural recording front-end is fully measured and characterized during both benchtop and *in vitro* experiments in saline.

ACKNOWLEDGMENT

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A High-Output-Impedance Current Microstimulator for Anatomical Rewiring of Cortical Circuitry

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Abstract—This paper reports on the design, implementation, and performance characterization of a high-output-impedance current microstimulator fabricated using the TSMC 0.35 μ m 2P/4M n-well CMOS process as part of a fully integrated neural implant for reshaping long-range intracortical connectivity patterns in an injured brain. It can deliver a maximum current of 94.5 μ A to the target cortical tissue with current efficiency of 86% and voltage compliance of 4.7V with a 5-V power supply. The stimulus current can be programmed via a 6-bit DAC with an accuracy better than 0.47 LSB. Stimulator functionality is also verified with *in vitro* experiments in saline using a silicon microelectrode with iridium oxide (IrO) stimulation sites.

I. INTRODUCTION

Throughout an individual's life, dendrites and spines branch and proliferate, synapses form and degenerate and the efficacy of synaptic contacts are modulated within a complex network of intracortical connections. Thus, it is not surprising that after an injury to cerebral cortex, the structure and function of these interconnected regions is drastically altered. Since plasticity may contribute to functional recovery after brain injury, it is critical to understand how plasticity patterns might be directed to optimize recovery.

Over the past few years, a large number of studies have contributed to the rationale behind this work [1]. First, substantial local axonal sprouting spontaneously occurs in the intact tissue adjacent to a focal cortical insult. This sprouting is limited to 1-2mm, and is thought to be guided by temporally-programmed waves of growth-promoting and -inhibiting proteins. Second, recent studies have demonstrated that long-range axonal sprouting too occurs spontaneously after focal cortical injury. In a non-human primate model of injury and recovery, the premotor hand area was found to send axons to a completely novel cortical target within the somatosensory cortex, a distance of more than 1cm [2]. Third, functional relationships can be built in the intact adult nervous system by artificially driving temporal sequences of inputs and outputs of cortical modules, at least over short distances. It has recently been demonstrated in intact primates that action potentials recorded from one cortical module can be used to drive microstimulation of another cortical module that is located 1-2mm away. Following several weeks of entrainment, the

two disparate modules had similar output properties [3].

We aim to develop a fully integrated neural implant, as shown schematically in Fig. 1, to temporally couple the activity of remote cortical locations that are not normally co-activated or interconnected [4]. The system consists of a low-noise front-end amplifier and a successive approximation register (SAR) ADC to record and digitize the extracellular neural data. An on-chip digital signal processing unit performs additional filtering and executes a spike discrimination algorithm to identify large single-unit action potentials that will be used for triggering a back-end intracortical microstimulator to deliver precisely controlled current pulses to the target cortical tissue.

We hypothesize that such temporal coupling encourages growing axons to migrate toward and terminate in the coupled region, as conceptually illustrated in Fig. 2. This paper presents the design, implementation, and preliminary measurement results for our first-generation back-end microstimulator of Fig. 1.

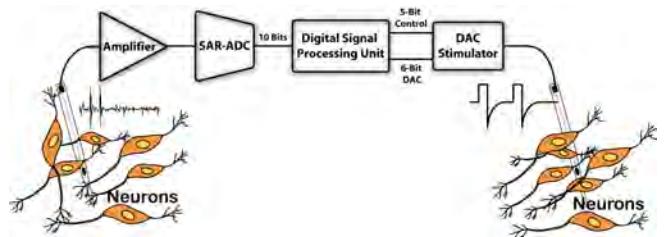


Figure 1. Schematic block diagram of the proposed integrated neural implant for activity-dependent intracortical microstimulation.

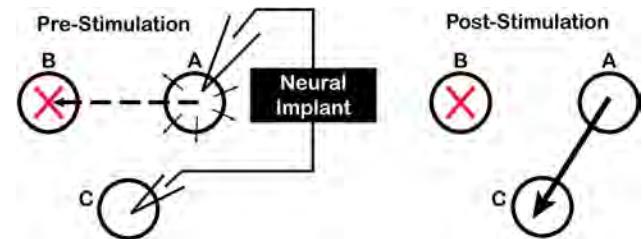


Figure 2. Hypothetical effects of activity-dependent stimulation on long-range intracortical connectivity. Left: After injury to B, normal connections are lost (dashed arrow). Post-injury growth proteins induce local axonal sprouting (short arrows). Neural implant will drive synchronous activity between A and C. Right: New anatomical connections form between A and C.

II. OUTPUT-IMPEDANCE-BOOSTED CURRENT MIRROR

A. Feedback Amplifier

To maintain a constant stimulus current regardless of the site and tissue impedances, a current source with high output impedance is required [5]. This will also facilitate maintaining charge balance in biphasic current stimulation. To achieve high output impedance values, long-channel transistors in cascode topology can be used as schematically depicted in Fig. 3(a). On the other hand, to maintain voltage compliance as close to the power supply as possible both output transistors in Fig. 3(a) must have large channel widths for a small overdrive voltage, leading to large silicon areas for on-chip implementation as well as slow step response.

As shown in Fig. 3(b), active feedback can be employed to boost the output impedance by nearly maintaining the same V_{ds} across transistors $M_{1,3}$. It can be shown that the output resistance of the current source in Fig. 3(b) is equal to:

$$R_{out} = A \times r_{o1} \times g_{m2} \times r_{o2} \quad (1)$$

where A is the amplifier voltage gain, r_{o1} is the output resistance of M_1 , and r_{o2} and g_{m2} are the output resistance and transconductance of M_2 , respectively. The voltage compliance of the current source can be calculated as:

$$V_{Compl} = V_{bp} + |V_{gs4}| - V_{OD2} \quad (2)$$

where V_{gs4} is the gate-source voltage of M_4 and V_{OD2} is the overdrive voltage of M_2 . As predicted by (2), V_{bp} should be increased to maintain high voltage compliance. However, increasing V_{bp} arbitrarily can drive M_1 into triode region, significantly degrading the output impedance. The optimum value for V_{bp} is $V_{dd} - |V_{gs4}| - V_{OD1}$, resulting in a voltage compliance of $V_{dd} - V_{OD2} - V_{OD1}$. The feedback amplifier must tolerate high input common-mode voltages, and provide adequate gain to achieve high output impedances. A single-stage folded-cascode topology with NMOS input transistors has been utilized for the feedback amplifier as shown in Fig. 4. The bias currents are designed for the amplifier to exhibit adequate gain and speed. A compensation capacitor limits the amplifier bandwidth for stability. Large compensation capacitors result in a very slow settling time for the output current, whereas small compensation capacitors can produce significant undesired ringing in the output current step response [6].

B. Impact Ionization Effect

When the source-drain voltage across the cascaded transistor M_2 (V_{sd2}) in the current mirror (with or without feedback circuitry) is high, a very high longitudinal electric field will be generated in the transistor channel. The maximum electric field occurs at the drain, and is a strong function of channel length and V_{ds} . If the maximum field is

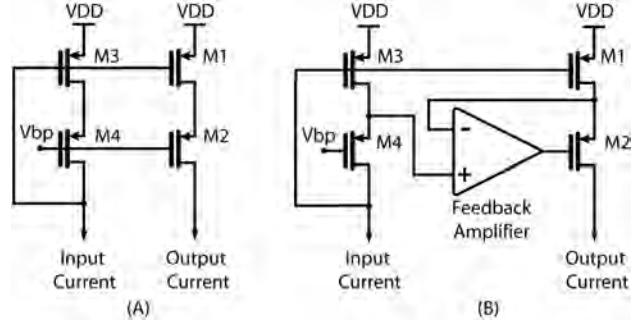


Figure 3. a) A two-transistor cascode current mirror. b) A current mirror with boosted output impedance via active feedback.

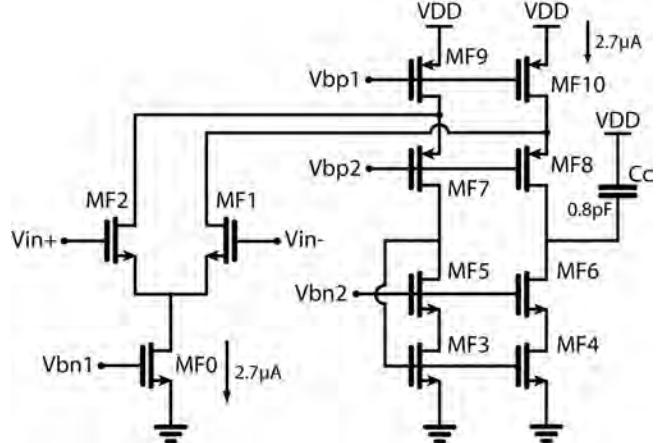


Figure 4. Transistor schematic of the feedback amplifier.

high enough, some of the electrons inside the channel acquire enough energy to impact the crystal lattice and create new electron-hole pairs. This effect is known as *impact ionization* and is further exacerbated in submicron processes with small channel length values [7]. The depletion region in the channel underneath the drain will push some of the electrons toward the substrate, generating a drain-bulk current, I_{db} . If the substrate of M_2 is tied to V_{dd} (or ground in case of an NMOS transistor), I_{db} cannot be controlled through feedback circuitry and the output current increases as the output voltage goes below a certain value, as simulated in Fig. 5. However, if the substrate of M_2 is connected to its source, then the extra current can be compensated by the feedback circuitry and the output current will not change significantly.

III. MICROSTIMULATOR ARCHITECTURE

The intracortical microstimulator is designed to deliver a constant current between 0 and $94.5\mu\text{A}$ in steps of $1.5\mu\text{A}$ (6-bit resolution) to the neural tissue in bipolar fashion during the first phase of stimulation. In the subsequent phase, the two stimulator output pins are shorted together by variable on-chip resistors to discharge the electrode-tissue interface capacitance. To accommodate the voltage drop across the cortical tissue, thick-oxide 5-V transistors are employed in the stimulator design. Figure 6 shows a schematic diagram of the microstimulator architecture.

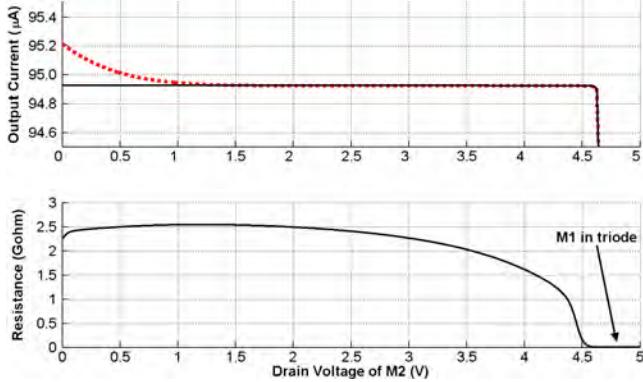


Figure 5. a) Simulated output current in Fig. 3(b) with the substrate of M₂ tied to its source (solid line) and to V_{dd} (dotted line). b) Simulated output resistance with the substrate of M₂ tied to its source.

A 6-bit current-based DAC generates a fraction (1/15) of the output current, which is then multiplied by a PMOS current mirror with its output impedance boosted by the feedback amplifier. The generated output current can be delivered to a bipolar stimulating electrode with two different polarities controlled by on-chip switches (S₁₋₄). Two switches, S₈₋₉, have also been added to turn the output current on/off. These switches in conjunction with the compensation capacitor (C_C = 0.8pF) enable a very fast step response for the current source with sub-microsecond rise and fall time. Following a constant current phase, switches S₅₋₇ short the stimulation sites together via three on-chip resistors.

Five externally applied control signals manage the stimulator operation modes via an on-chip control unit. To operate with a low-power low-voltage digital unit, all control signals as well as DAC inputs are activated with 2V. In standby mode (when control bit *Mode-0* is low), the internal circuitry is powered down and the two output pins (PIN-1 and PIN-2) are in high impedance state. During the first phase of stimulation, constant current will flow from PIN-1 (PIN-2) towards PIN-2 (PIN-1) depending on the status of the control bit *Mode-1*. In the subsequent phase (when control bit *EN* is low), the two output pins are shorted together by a combination of on-chip resistors programmable via the remaining two control bits *RES-1* and *RES-2*. Table I summarizes the stimulator operation modes.

TABLE I

MICROSTIMULATOR OPERATION MODES

CONTROL BITS: Mode-0 Mode-1 EN RES-1 RES-2

INPUT	OPERATION MODE
0xxxx	Standby- Internal circuitry is powered down
101xx	Constant current flows from PIN-1 \Rightarrow PIN-2
111xx	Constant current flows from PIN-2 \Rightarrow PIN-1
1x000	Shorted output pins w/ 48-kΩ resistor (R ₁)
1x001	Shorted output pins w/ 16-kΩ resistor (R ₁ R ₂)
1x010	Shorted output pins w/ 9.6-kΩ resistor (R ₁ R ₃)
1x011	Shorted output pins w/ 6.8-kΩ resistor (R ₁ R ₂ R ₃)

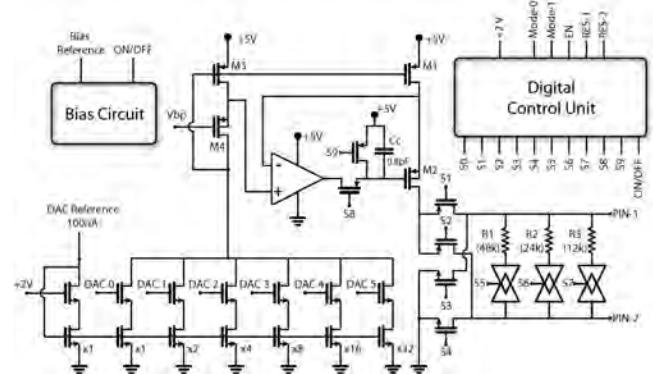


Figure 6. Schematic diagram of the current-based cortical stimulator.

IV. MEASUREMENT RESULTS

A prototype microstimulator was fabricated using the TSMC 0.35μm 2P/4M n-well CMOS process on a 2.6 × 2.6-mm² integrated circuit that also incorporated two different versions of the front-end recording circuitry of Fig. 1. Figure 7 shows a microphotograph of the fabricated chip. The stimulator occupied a silicon area of 200μm × 110μm. With the DAC input code equal to zero (i.e., zero output current), the stimulator consumed 45μW from a 5-V supply. When delivering the maximum current (i.e., measured current of ~94μA), the stimulator had a current draw of ~110μA.

Figure 8 shows the measured stimulus output current versus the output voltage for four different DAC input values. Voltage compliance at maximum deliverable current was measured to be 4.7V, which is 94% of the supply voltage. The measured output impedance was beyond our testing equipment accuracy (> 45MΩ), but the simulation results predicted an output impedance of ~1GΩ. Figure 9 shows the measured stimulus output current versus the DAC input codes. The DAC was found to have a measured integral nonlinearity (INL) between ±0.47 LSB (±0.7μA).

To further characterize the stimulator performance, it was interfaced with a microfabricated silicon electrode (the so-called Michigan probe [8]) for *in vitro* experiments in saline.

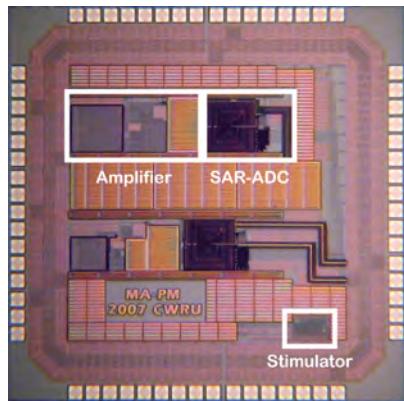


Figure 7. Microphotograph of the fabricated chip.

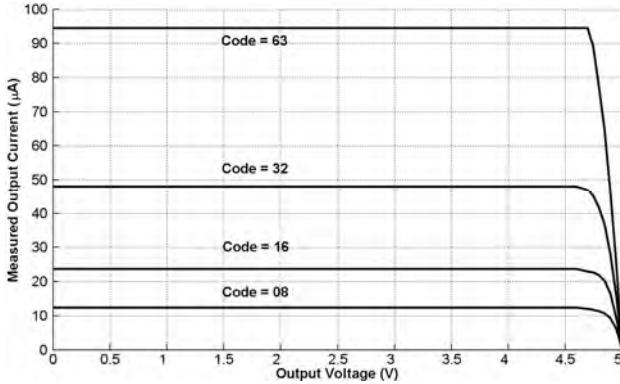


Figure 8. Measured stimulus output current versus the output voltage for four different DAC input values.

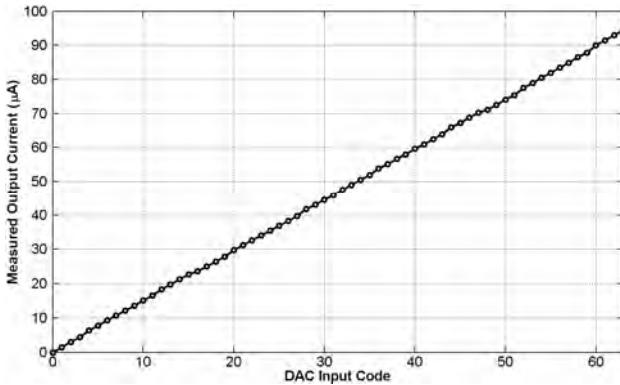


Figure 9. Measured stimulus output current versus DAC input codes.

The probe incorporated five stimulation sites of iridium oxide (IrO), linearly spaced apart on a 1-mm silicon shank. Bipolar stimulation between two adjacent sites was performed with a $2\text{-k}\Omega$ resistor externally connected in series with the probe to measure the stimulus current flowing between the two sites. The measured stimulus current and the site voltage are plotted versus time in Fig. 10. Table II summarizes the measured performance specifications of the microstimulator.

TABLE II

MICROSTIMULATOR PERFORMANCE SUMMARY

Technology	$0.35\text{-}\mu\text{m}$ 2P/4M CMOS
<u>Output Impedance</u>	
Simulation	$1\text{G}\Omega$
Measurement	$> 45\text{M}\Omega$
Max. Stimulus Current	$94.5\mu\text{A}$
DAC Linearity	$< \pm 0.47 \text{ LSB} (< \pm 0.7\mu\text{A})$
Voltage Compliance	4.7V ($I_{\text{out}} = 94.5\mu\text{A}$)
Stimulus Current Rise Time (0 to 90% Settling Time)	$< 1\mu\text{s}$ $I_{\text{out}} = 94.5\mu\text{A}$ delivered to $10\text{k}\Omega$
Power Consumption (@ 5V)	$45\mu\text{W}$ ($I_{\text{out}} = 0$) $< 5\mu\text{W}$ (Standby)
Current Efficiency	86% ($I_{\text{out}} = 94.5\mu\text{A}$)
Silicon Area	$200\mu\text{m} \times 110\mu\text{m}$

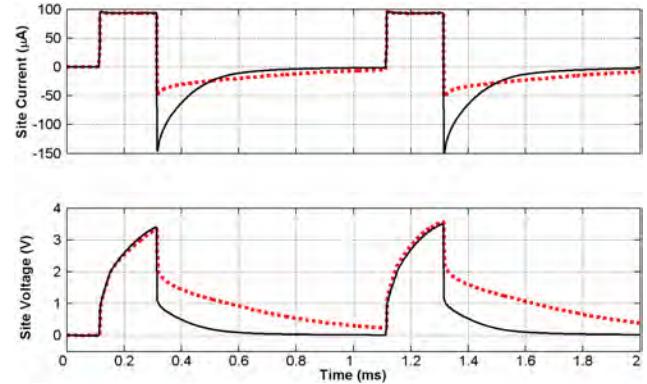


Figure 10. Measured stimulus current (top) and site voltage (bottom) during *in vitro* experiments with the microstimulator interfaced with a silicon-substrate Michigan probe. The DAC input code and the time duration of the *EN* signal were set to 63 and $200\mu\text{s}$, respectively. Solid line corresponds to an electrode shorting case with a $6.8\text{-k}\Omega$ on-chip resistor ($\text{RES-1 RES-2} = 11$), whereas the dashed line corresponds to electrode shorting with a $48\text{-k}\Omega$ on-chip resistor ($\text{RES-1 RES-2} = 00$).

V. CONCLUSION

We are developing a fully implantable microsystem for activity-dependent microstimulation in order to reshape long-range intracortical connectivity patterns in an injured brain. This paper reports on a programmable high-output-impedance microstimulator fabricated in a $0.35\text{-}\mu\text{m}$ CMOS process employing thick-oxide transistors. It can deliver up to $94.5\mu\text{A}$ with current efficiency of 86% from a 5-V power supply for bipolar stimulation. Stimulator functionality has also been verified with *in vitro* experiments in saline using a silicon microelectrode with stimulation sites of iridium oxide.

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Appendix III M. Roham, J. M. Halpern, H. B. Martin, H. J. Chiel, and P. Mohseni, "Wireless amperometric neurochemical monitoring using an integrated telemetry circuit," *IEEE Trans. Biomed. Eng.*, vol. 55, no. 11, pp. 2628-2634, November 2008.

Wireless Amperometric Neurochemical Monitoring Using an Integrated Telemetry Circuit

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Abstract—An integrated circuit for wireless real-time monitoring of neurochemical activity in the nervous system is described. The chip is capable of conducting high-resolution amperometric measurements in four settings of the input current. The chip architecture includes a first-order $\Delta\Sigma$ modulator ($\Delta\Sigma M$) and a frequency-shift-keyed (FSK) voltage-controlled oscillator (VCO) operating near 433 MHz. It is fabricated using the AMI 0.5 μm double-poly triple-metal n -well CMOS process, and requires only one off-chip component for operation. Measured dc current resolutions of ~ 250 fA, ~ 1.5 pA, ~ 4.5 pA, and ~ 17 pA were achieved for input currents in the range of ± 5 , ± 37 , ± 150 , and ± 600 nA, respectively. The chip has been interfaced with a diamond-coated, quartz-insulated, microneedle, tungsten electrode, and successfully recorded dopamine concentration levels as low as 0.5 μM wirelessly over a transmission distance of ~ 0.5 m in flow injection analysis experiments.

Index Terms—Amperometry, delta-sigma modulator, diamond microelectrode, dopamine, neurochemical monitoring, wireless integrated circuit.

I. INTRODUCTION

APID long-distance communication in the nervous system primarily occurs via electrical impulses. At the junctions between nerve cells, however, synapses communicate through the release and uptake of biochemical molecules called neurotransmitters [1], [2]. Elicted from the presynaptic neuron by the action potential, released neurotransmitter diffuses toward the postsynaptic neuron and binds to specific protein receptors, eliciting a change in the physiological status of the target neuron that ultimately determines the probability of whether a new action potential will be generated.

Abnormal variations of the physiological levels of neurotransmitters within the brain and nervous system have been

linked to several neurological disorders such as Alzheimer's and Parkinson's disease, and epilepsy [3]. Many neuroactive substances, such as therapeutic drugs (e.g., Zoloft) and drugs of abuse (e.g., cocaine) act by changing neurotransmitter levels at synapses, or by mimicking the actions of neurotransmitters at postsynaptic receptors. Moreover, much of the plasticity of the nervous system, which underlies learning and memory, is due to modifications of chemical synapses. Many of the biogenic aminergic systems, such as those that release dopamine or serotonin, provide outputs to large regions of the brain that affect mood, learning, and cognition [4]. Hence, understanding brain function on a fundamental level requires measurements of both electrical and chemical activity; this would provide a more holistic image of neural signal pathways, which might be of great benefit to physicians to better understand neuronal communication for more effective clinical treatments [5].

One major component of such technology for simultaneous monitoring and manipulation of electrical and chemical neural activity would be an electrode capable of both recording and stimulation. Implantable, biocompatible, robust, multifunctional microprobes capable of electrophysiological and chemical sensing in the brain must be developed. These implanted electrodes would monitor, e.g., the real-time extracellular concentration variations of neurotransmitters such as dopamine, a deficiency of which is found in patients with Parkinson's disease [6].

Another major component of such technology would be a low-power, multichannel, wireless microsystem that can be interfaced with the aforementioned electrodes to condition, process, and wirelessly transmit the recorded electrical and chemical neural signals from inside the body to the outside world. Wireless operation would eliminate the need for the cable link between the subject and the recording equipment, which is believed to adversely affect the behavior and to exclude experimental models involving complex or enriched environments [7], [8]. Very-large-scale integration (VLSI) using standard CMOS technology offers the potential for rapid, low-noise, multichannel, distributed sensing and measurement of electrical action potentials and neurochemical signals, using a low-power microsystem with a small form-factor suitable for long-term implantations.

This paper reports on developing sensor and wireless circuit technologies for neurochemical monitoring in the nervous system. Section II presents the development of diamond-coated microneedle electrodes for neurosensing, while Section III discusses the architecture of the wireless interface chip. Section IV presents detailed measurement results from benchtop and flow injection analysis experiments. Finally, Section V draws some conclusions.

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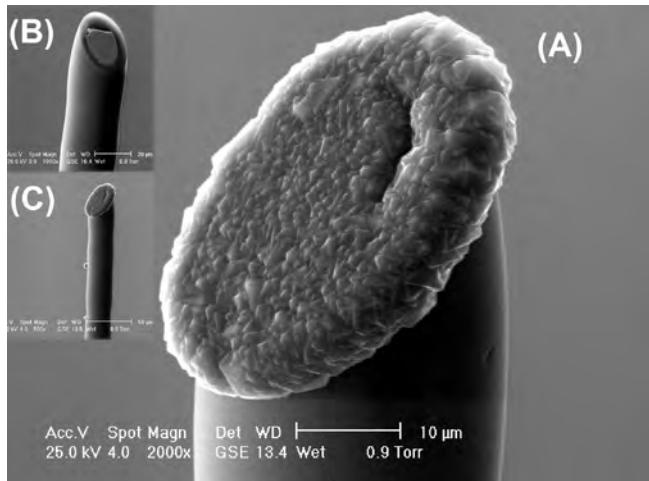


Fig. 1. SEM images of (a) and (c) selective diamond deposition on a (b) tungsten microelectrode; final tip diameter is 35 μm . Negligible diamond growth is observed on the walls of the quartz insulating capillary.

II. DIAMOND-COATED MICROELECTRODES

To analyze neurotransmitters by neurochemical monitoring, electrochemistry has been used as a rapid sensing technique that can directly detect electroactive neurochemical messengers. Electrochemistry involves bidirectional charge transfer between an electrode and a sample in solid or liquid phase, with the applied electrode potential providing energy for an electron transfer (i.e., a chemical reaction) to occur [9]. The chemical reactions occur at the electrode's surface or very short distances away within the probed sample volume, and the resulting charge transfer or current is measured. The measured current depends on the material properties and geometry of the electrodes as well as the concentration of the electroactive neurotransmitter, i.e., the target analyte. These techniques are attractive due to their high sensitivity, rapidity, and ability to perform distributed measurements.

For electrochemical detection of neurotransmitters, researchers have previously used gold electrodes, carbon-fiber microelectrodes, and microfabricated, screen-printed, polymer-modified carbon sensor arrays [10], [11]. Conductive diamond has emerged as a potentially superior electrode biomaterial. It is chemically and mechanically robust with a low baseline current, allowing long-term use and greater sensitivity for detecting lower analyte concentrations. The investigation of new chemistries is also possible due to diamond's wide-potential window of water stability. In addition, diamond's predictable surface chemistry discourages adsorption and oxygen reduction [12], [13].

In this paper, heavily conductive, boron-doped, polycrystalline diamond has been selectively deposited onto individual polished tips of tungsten microelectrodes, as shown in Fig. 1, using standard hot-filament chemical vapor deposition (CVD). Each tungsten microelectrode substrate was fabricated by presealing a tungsten microwire (25 μm diameter) into a pulled quartz capillary, and then, beveling at a 45° angle to form a coarsely polished elliptical disk. Polycrystalline

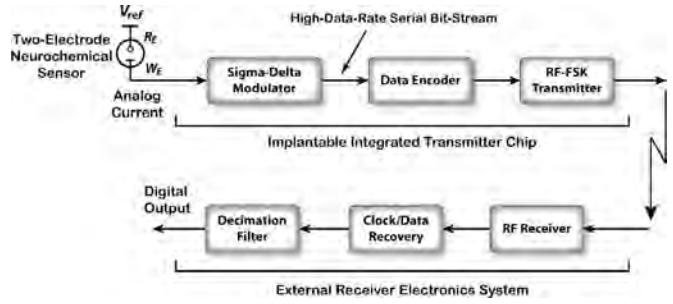


Fig. 2. Schematic block diagram of the wireless neurochemical sensing system, comprising an implantable integrated transmitter chip as well as external receiver electronics.

diamond was selectively deposited for up to 3 h in a standard methane/hydrogen/trimethylboron CVD environment at 20 torr [12], [14]. The novel needle-like geometry of these diamond microneedle electrodes mimics that of commercially available carbon- and metal-based microelectrodes, and enables implantation with minimal tissue damage. Using the diamond electrodes *in vitro*, biogenic amines have been electrochemically measured at millisecond time scales, e.g., serotonin in the vicinity of individual identified nerve cells in a marine mollusk *Aplysia californica* [15]; in this case, the diamond electrode also separately recorded neuroelectrical activity.

III. INTEGRATED CIRCUIT ARCHITECTURE

Since physiological concentrations of various neurotransmitters are on the order of nanomolar, the neurochemical sensing circuitry typically needs to be able to measure currents on the order of picoamperes to nanoamperes, based on the transduction characteristics of a particular sensor. At the same time, current resolution levels of a few picoamperes might be required. Single- and multichannel integrated interface circuits for amperometric electrochemical biosensors [16]–[21] as well as for cell-based electrophysiological studies in patch-clamp applications [22] have been previously reported. In this paper, an integrated circuit for low-noise current measurements via an active wireless link has been developed that, compared to any previous reports, simultaneously achieves high current resolution and fast conversion speed in four wide-dynamic-range input current settings. This performance is primarily achieved by employing low-noise front-end design techniques on the transmitter side as well as efficient off-chip digital filtering on the receiver side.

Fig. 2 depicts the architecture of the proposed wireless neurochemical recording system, comprising an implantable integrated transmitter chip as well as external receiver electronics. On the transmitter side, the analog input current is directly converted to a serial data bit stream using an on-chip, first-order, current-input, $\Delta\Sigma$ modulator ($\Delta\Sigma M$). A low-power radio-frequency (RF) transmitter then sends the resulting digital data to the outside world at a carrier frequency near 433 MHz after Manchester encoding.

The direct conversion of the analog input current to a digital output bit stream alleviates the need for conventional current-to-voltage (I/V) converters based on operational amplifiers and

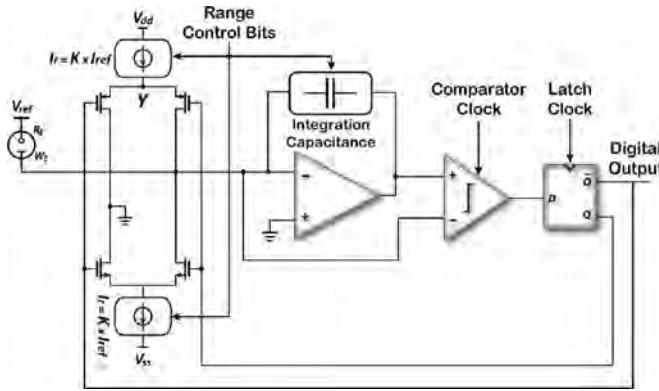


Fig. 3. Schematic block diagram of the current-input, first-order, front-end $\Delta\Sigma$ modulator.

resistors that can be inherently noisy and nonlinear, and thus unsuitable for low-current sensing applications.

On the receiver side, the encoded data are extracted using a commercially available, wideband, RF-to-IF₂ down-converter followed by custom electronics for IF₂-to-baseband conversion. The IF₂ filter bandwidth is ± 5 MHz centered around 10.7 MHz. Next, a Manchester decoder recovers the original clock and data signals, and a software-based decimation filter provides the final high-resolution digital output.

In this design, the decimation filter for the $\Delta\Sigma$ M is implemented in software on the receiver side. Since the entire digital filtering stage is transferred from the on-chip implantable side to the external receiver side, significant reductions in silicon area and power consumption can be achieved. Moreover, the built-in flexibility of software implementation for the decimation filter allows one to dynamically tradeoff between the required resolution and data conversion speed.

A. Current-Input First-Order $\Delta\Sigma$ Modulator

Fig. 3 shows the schematic block diagram of the low-power, low-noise, first-order $\Delta\Sigma$ M that lies at the core of the current-measuring circuitry. A two-stage operational amplifier featuring a simulated gain-bandwidth product of 1.9 MHz and a phase margin of 68° is used in the integrating stage. It consumes ~ 10 μ A from a 2.6-V power supply. A 5- μ W, clocked, binary comparator digitizes the analog output of the integrating stage with a sampling frequency of 130 kHz. The latching clock is delayed by 22.5° with respect to the comparator clock in order to allow the data to settle prior to latching. In this architecture, reference current sources are the main contributors to the input-referred noise. The current source transistors are laid out as wide-channel matched transistors in a 2-D common-centroid topology to reduce the input-referred offset current and noise that can directly corrupt very-low-current measurements.

The $\Delta\Sigma$ M is designed to operate in four different regions depending on the input current dynamic range. Region A corresponds to the maximum dynamic range of ± 600 nA (i.e., $\pm I_{\text{ref}}$). Regions B, C, and D correspond to input current dynamic ranges of ± 150 , ± 37.5 , and ± 4.7 nA, respectively. In order to maintain

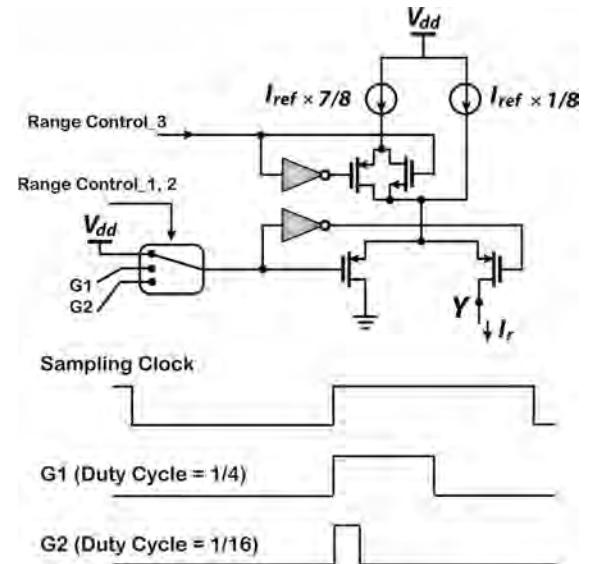


Fig. 4. Illustration of range selection mechanisms. (Top) Circuitry for scaling I_{ref} . (Bottom) G_1 and G_2 signals drawn with respect to the sampling clock for modulating the duty cycle of I_{ref} in method (2). Sampling occurs at the negative edges.

a constant sampling frequency, range changes can be accomplished by scaling the reference current I_{ref} and the integrating capacitance using externally applied range control bits. The reference current can be scaled down by either: 1) switching in smaller current sources (e.g., a fraction of the original I_{ref}) or 2) modulating the duty cycle of I_{ref} in each sampling cycle to reduce its effective value [19], [20]. It should be noted, however, that method (1) cannot be employed arbitrarily, because the achievable offset and noise performances of very-low-amplitude matched current sources are largely process-dependent. As a result, a combination of the two techniques is employed as schematically depicted in Fig. 4 and tabulated in Table I.

The 600-nA reference current I_{ref} is divided into two smaller current sources of $0.125 \times I_{\text{ref}}$ and $0.875 \times I_{\text{ref}}$. For operation in Region A, both current sources are switched in and no modulation of the duty cycle is performed. For operation in Regions B and C, both current sources are switched in again and duty cycle modulations of 25% and 6.25% are applied, respectively. For operation in Region D, only the smaller current source (i.e., $0.125 \times I_{\text{ref}}$) is switched in with a duty cycle modulation of 6.25%. The integration capacitance is divided into four parts as well and switched in according to the operation region, as also summarized in Table I. The $\Delta\Sigma$ M occupies an active area of $420 \mu\text{m} \times 210 \mu\text{m}$ in a 0.5- μm CMOS process and consumes 22 μA from a 2.6-V supply.

B. RF Transmitter

A cross-coupled voltage-controlled oscillator (VCO) circuit for analog frequency-modulated data transmission has been previously reported in [23]. In this paper, we use a similar design with a different tuning scheme for digital frequency-shift-keyed (FSK) transmission, as shown schematically in Fig. 5. The oscillator tank employs a surface-mount, high- Q , off-chip inductor

TABLE I
SUMMARY OF RANGE SELECTION MECHANISMS

Region	K^*	$I_{ref} \times 1/8$ Switched in	$I_{ref} \times 7/8$ Switched in	Duty Cycle Modulation (G_1)	Duty Cycle Modulation (G_2)	Integration Capacitance
A	1	✓	✓	-	-	8pF
B	1/4	✓	✓	✓	-	2pF
C	1/16	✓	✓	-	✓	0.5pF
D	1/128	✓	-	-	✓	80fF

* See Fig. 3.

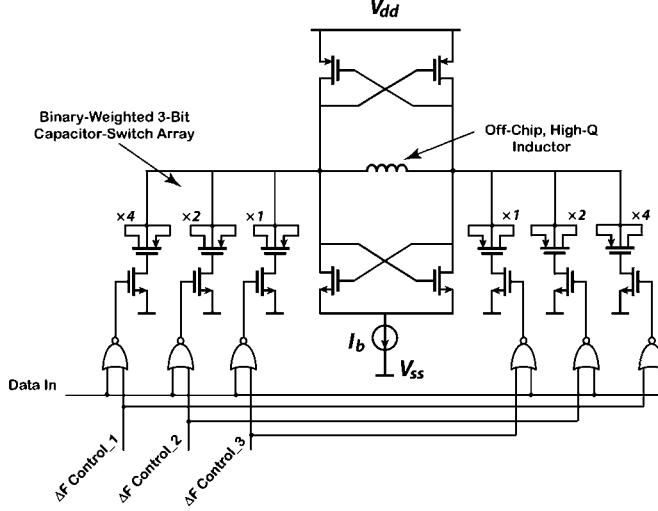


Fig. 5. Transistor-level circuit schematic of the cross-coupled VCO for FSK transmission.

for low-power operation at a frequency near 433 MHz. The tank switched capacitors are implemented using positive-channel MOS (PMOS) transistors with source/drain/bulk connected to each other. Flexibility in selecting a suitable ΔF for the FSK transmitter is achieved by dividing the capacitors into two sets of binary-weighted elements that can be externally controlled with 3 bits. The negative-channel MOS (NMOS) control switches are optimally sized to reduce their resistance and parasitic capacitance. Using this tuning scheme, ΔF can be varied in the range of 2–14 MHz in steps of 2 MHz. The transmitter bias current I_b is externally controllable in the range of 100–500 μ A. The VCO occupies an active area of 175 μ m \times 65 μ m in a 0.5- μ m CMOS process.

IV. MEASUREMENT RESULTS

A. Benchtop

A prototype integrated circuit was fabricated using the AMI 0.5 μ m double-poly triple-metal n-well CMOS process, and measured 2.2 mm \times 2.2 mm including the bonding pads. Fig. 6 shows a microphotograph of the fabricated chip. The chip was fully characterized for functionality during benchtop tests using a *Keithley 6221* dc/ac current source [24].

Fig. 7 shows the wirelessly measured dc characteristics of the system with the input current varying in the range of 500 fA–600 nA in both positive and negative directions. The system achieved a highly linear response over six decades of the input

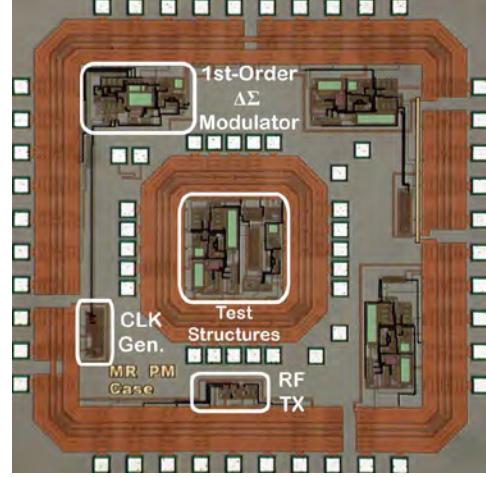


Fig. 6. Microphotograph of the 2.2 mm \times 2.2 mm chip fabricated using the AMI 0.5 μ m 2P/3M n-well CMOS process.

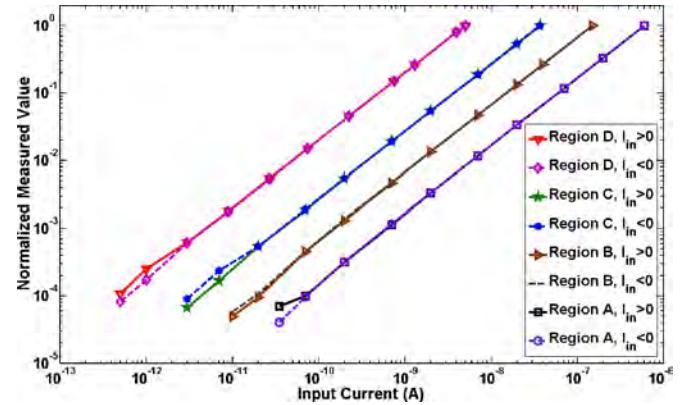


Fig. 7. Wirelessly measured dc characteristics of the system with input current in the range of 500 fA–600 nA. Measured values in each region are normalized to the maximum value of the corresponding region (i.e., 600 nA, 150 nA, 37 nA, 5 nA for regions A, B, C, and D, respectively). High linearity is achieved over six decades of the input current.

current. DC current resolutions of \sim 17 pA, \sim 4.5 pA, \sim 1.5 pA, and \sim 250 fA were achieved in regions A, B, C, and D, respectively. In this test, the digital output of the system was decimated to 100 Hz at the receiver, and 100 samples were averaged per second to produce a dc current value. Current resolution in each operation region was reported as the measured peak noise on the resulting output current when the input current was lowered to a minimum value that could be measured with an error less than 50%. For example, in region D, the system was able to

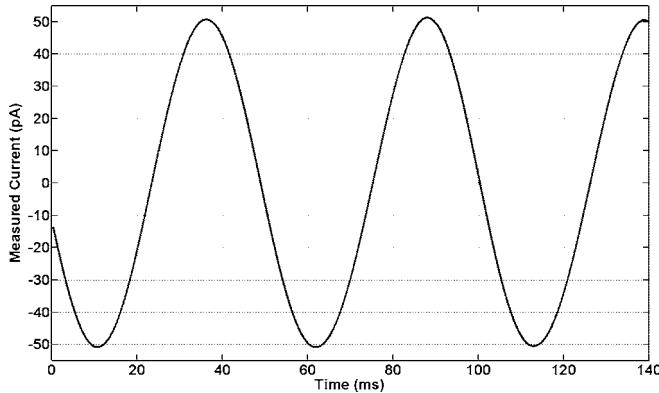


Fig. 8. Wirelessly measured ac response of the system with a 20-Hz, 100-pA_{pp} sinusoidal input current. The recorded signal shown herein is input-referred. The chip is programmed to operate in region D (± 5 nA).

measure a minimum input current of 500 fA with a resolution of ± 250 fA.

Fig. 8 shows the system ac response for a 20-Hz, 100-pA_{pp} sinusoidal input current measured wirelessly at 430 MHz with the chip set to operate in region D (± 5 nA). The decimation filter bandwidth was set to 50 Hz on the receiver side.

B. Flow Injection Analysis

For neurotransmitter monitoring in flow injection analysis experiments, the fabricated CMOS chip was interfaced with a diamond-coated microprobe as the working electrode (W_E). All measurements were collected in buffer containing 150 mM NaCl and 20 mM HEPES (pH = 7.4). The electrode was placed in a flow cell and buffer pumped at a rate of 2 mL/min. A bolus of dopamine at different concentrations was applied to the flowing stream via a loop injector driven by a pneumatic actuator.

A custom-written LabVIEW program was developed to apply the oxidation-reduction (redox) potential and initiate a chemical reaction. A chloridized silver wire (Ag/AgCl) was used as a standard electrochemical reference electrode (R_E). The resulting current generated at the diamond electrode surface was then wirelessly reported by the chip. The redox potential was chosen where the oxidation current for dopamine was maximum, determined prior to this experiment by fast-scan cyclic voltammetry at the same diamond electrode. For all flow cell experiments, the chip was set to operate in region D (± 5 nA).

Fig. 9 depicts the static calibration curve (current versus dopamine concentration) obtained in the flow cell for an applied potential of ~ 0.8 V versus Ag/AgCl where dopamine oxidation will occur. Dopamine concentration levels of 0.5, 2, 6.5, 10, 20, and 30 μ M were applied. As can be seen, a highly linear response was achieved in a truly wireless measurement. Fig. 10 shows the dynamic plot (dopamine current versus time) with a dopamine concentration level of 20 μ M injected into the flow cell.

The rise and fall time instances within this temporal profile correspond to when dopamine injection was turned ON and OFF, respectively (i.e., 15 s bolus); these timestamps are offset from

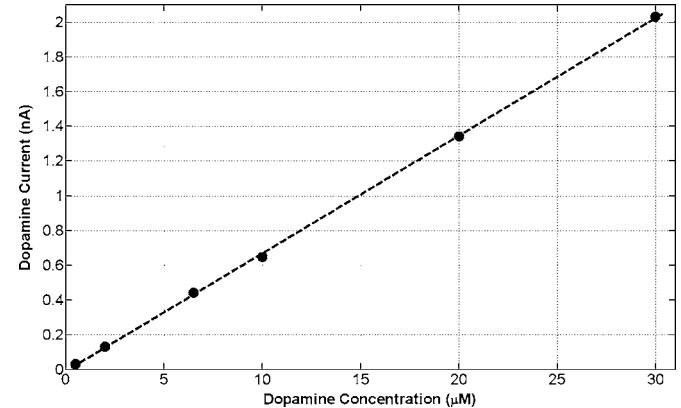


Fig. 9. Wirelessly measured static calibration curve (current versus dopamine concentration). Dopamine concentration levels of 0.5, 2, 6.5, 10, 20, and 30 μ M in an HEPES buffer are applied in the flow cell. The applied potential is ~ 0.8 V versus Ag/AgCl.

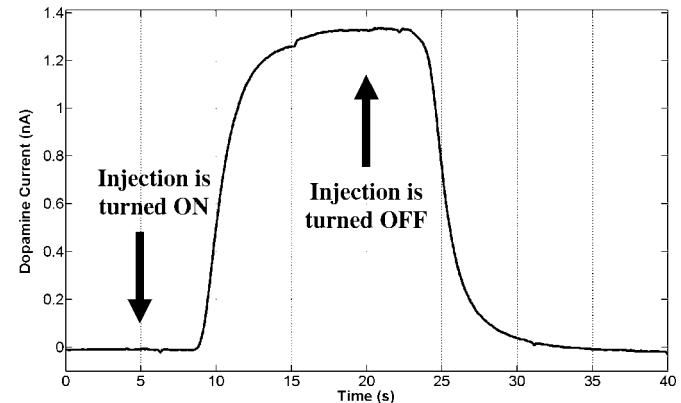


Fig. 10. Wirelessly measured 20 μ M dopamine current after 40 s of amperometry in flow injection analysis experiments. The current is measured in an HEPES buffer at the applied potential of ~ 0.8 V versus Ag/AgCl.

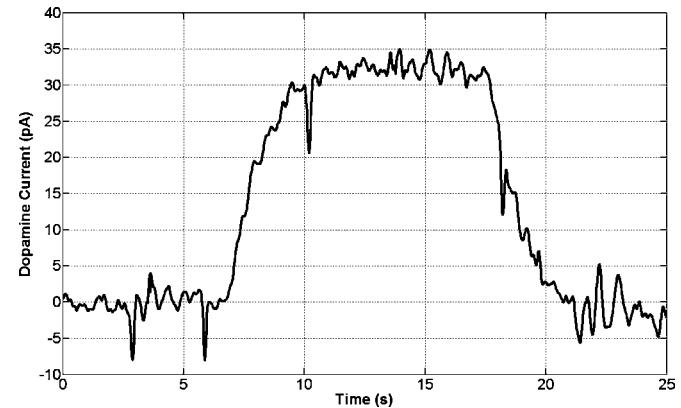


Fig. 11. Wirelessly measured 0.5 μ M dopamine current after 25 s of amperometry in flow injection analysis experiments. The current is measured in an HEPES buffer at the applied potential of ~ 0.8 V versus Ag/AgCl.

the actual increase and decrease of dopamine due to an inherent lag in the flow cell before electrolyte reaches the electrode.

Finally, Fig. 11 depicts the same plot with dopamine concentration level of 0.5 μ M injected into the flow cell, resulting in a measured peak dopamine current of ~ 33 pA. Table II summarizes the measured performance of major circuitry and Table III

TABLE II
SUMMARY OF MEASURED PERFORMANCE CHARACTERISTICS

AΣ Modulator Sampling Rate	130kHz
Decimated Sampling Rate	100Hz
Measured DC Current Resolution**	
Region A ($\pm 600\text{nA}$)	$\sim 17\text{pA}$
Region B ($\pm 150\text{nA}$)	$\sim 4.5\text{pA}$
Region C ($\pm 37\text{nA}$)	$\sim 1.5\text{pA}$
Region D ($\pm 5\text{nA}$)	$\sim 250\text{fA}$
Communication Scheme	FSK @ 433MHz
RF Data Transmission Rate	260kb/s (Encoded)
Received Power at 0.5m	-60dBm (w/ 5-cm monopole TX and 50-cm RX antennae)
Power Supply	$\pm 1.3\text{V}$
Power Consumption / Active Area	
Sensor Interface (ADC)	$\sim 57\mu\text{W} / 420\mu\text{m} \times 210\mu\text{m}$
RF Transmitter	$\sim 1\text{mW} / 175\mu\text{m} \times 65\mu\text{m}$
Technology	AMI 0.5μm 2P3M n-well CMOS

** See Section IV-A.

TABLE III
RECORDING CHIP PERFORMANCE COMPARISON

	This Work	[18]	[19]
Neurochemical Sensing Modality	Amperometry	Amperometry	Amperometry
# of Channels	1	16	16
Communication Scheme	FSK (Uplink)	Wired	Wired
Power Supply	$\pm 1.3\text{V}$	-2V; 7V	3V
Current Resolution	$\sim 250\text{fA}^{**}$ in $\pm 5\text{nA}$ $\sim 1.5\text{pA}^{**}$ in $\pm 37\text{nA}$ $\sim 17\text{pA}^{**}$ in $\pm 600\text{nA}$	46pA in $\pm 50\text{nA}$ 1nA in $\pm 500\text{nA}$ (12-kHz BW)	100fA in $\pm 8\text{pA}$ ($< 0.1\text{-Hz BW}$) 15.3pA in $\pm 500\text{nA}$ (15-Hz BW)
Power Consumption (per channel)	$57\mu\text{W}$	$780\mu\text{W}$	$4.3\mu\text{W}$ ($\pm 8\text{pA}$ Range) $48.3\mu\text{W}$ ($\pm 500\text{nA}$ Range)
Technology	0.5μm CMOS	1.2μm BiCMOS	0.5μm CMOS

** See Section IV-A.

compares the overall chip performance with that in recent published work.

V. CONCLUSION

In this paper, we reported on technology development at the sensor and circuit levels for wireless neurochemical monitoring using amperometry. Robust, versatile, implantable, microneedle electrodes were fabricated by chemical vapor deposition of highly conductive diamond onto the polished tip of a tungsten microelectrode. Moreover, integrated CMOS electronics were developed for conditioning and wirelessly transmitting the electrochemical signals corresponding to extracellular concentration variations of target neurotransmitters. Dopamine, a major electroactive neurotransmitter, with concentration levels as low as $0.5\text{ }\mu\text{M}$ was wirelessly recorded in flow cell by interfacing the diamond microelectrodes with the CMOS microelectronics.

ACKNOWLEDGMENT

The design, implementation, testing, and characterization of the integrated circuit were performed in the Electrical Engineering and Computer Science Department, Case Western Reserve University (CWRU), Cleveland, OH 44106 USA, and the dia-

mond electrode development and flow injection analysis experiments were conducted in the Chemical Engineering Department at CWRU.

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Appendix IV D. J. Guggenmos, S. Barbay, P. Mohseni, and R. J. Nudo, "A comparison of monopolar and bipolar electrodes for use in intracortical microstimulation," *Program No. 101.23, Neuroscience Meeting Planner*, Washington, DC, Society for Neuroscience, November 2008.

